PROGRAMMABLE ON CHIP REGULATORS WITH BYPASS

ABSTRACT OF THE DISCLOSURE

A device and a method for processing high data rate serial data includes circuitry for recovering or generating a clock based with varying amounts of phase noise or jitter based upon a particular application. To achieve the foregoing, regulated and unregulated power are selectively provided to the circuitry for recovering a clock, to the circuitry for generating a transmission clock, and to any other circuitry having different tolerance levels for jitter and phase noise. Each power regulator comprises a current supply module and voltage regulator module. The current supply module provides one of a plurality of selectable output current levels into an output node of the regulator. The voltage regulator module having selectable voltage divider ratios at a first input of a comparator regulates an amount of current the device sinks from the output node to adjust the output voltage.